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What is claimed is:

1. An amplifier comprising:

a first stage having at least two power states, said first stage having an input for receiving a data signal, a control port, and an output;

a second stage having at least two power states, said second stage having an input coupled to the output of said first stage, a control port, and an output; and

a state determination circuit coupled to the control port of said first stage for selectively configuring said first stage in one of the at least two power states and further coupled to the control port of said second stage for selectively configuring said second stages in one of the at least two power states.

2. The amplifier of claim 1, further comprising an output impedance matching circuit having at least two impedance matching states, said output impedance matching circuit having an input coupled to the output of said second stage, a control port, and an output for coupling to a load, said state determination circuit further for selectively configuring said output impedance matching circuit in one of the at least two impedance matching states.

3. The amplifier of claim 2, wherein said sate determination circuit selectively configures said first stage, said second stage, and said output impedance matching circuit such that said amplifier operates at a first power level when an output power level is within a first range and a second power level when the output power level is within a second range.

4. The amplifier of claim 2, wherein said first stage comprises at least:

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a first power device; and

a second power device connected in parallel with said first power device.

5. The amplifier of claim 4, wherein said second stage comprises at least:

a third power device; and

a fourth power device connected in parallel with said first power device.

6. The amplifier of claim 5, wherein said state determination circuit selectively configures said first stage by selectively enabling said second power device, said first stage being in a first of the at least two power states when said first and second power devices are enabled and being in a second of the at least two power states when said first power device is enabled and said second power device is not enabled; and

wherein said state determination circuit selectively configures said second stage by selectively enabling said fourth power device, said second stage being in a first of the at least two power states when said third and fourth power devices are enabled and being in a second of the at least two power states when said third power device is enabled and said fourth power device is not enabled.

7. The amplifier of claim 6, wherein:

said at least two power states of said first stage consists of said first and second of the at least two power states of said first stage;

said at least two power states of said second stage consists of said first and second of the at least two power states of said second stage; and

said amplifier is in a first power level when said first and second stages are in said first of their at least two power states and is in a second power level when said first and second stages are in said second of their at least two power states.

8. The amplifier of claim 5, wherein said first, second, third, and fourth power devices are transistors.

9. The amplifier of claim 2, further comprising an interstage impedance matching circuit coupled between the output of said first stage and the input of said second stage.

10. The amplifier of claim 2, further comprising an input stage impedance matching circuit coupled to the input of said first stage, said signal being received through said input stage matching circuit.

11. The amplifier of claim 2, wherein said output impedance matching circuit comprises:

a first transmission line having a first end coupled to the output of said second stage and further having a second end;

a second transmission line having a first end coupled to the output of said second stage and further having a second end; and

a diode having an anode coupled to the second end of said first transmission line and a cathode coupled to the second end of said second transmission line.

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12. The amplifier of claim 2, wherein said output impedance matching circuit comprises:

a transmission line having a first end coupled to the output of said second stage and further having a second end;

a capacitor having a first end coupled to ground and further having a second end; and

a diode having an anode coupled to the second end of said transmission line and a cathode coupled to the second end of said capacitor.

13. A wireless device including an amplifier, said wireless device capable of establishing communication with a base station, said amplifier comprising:

a first stage having at least two power states, said first stage having an input for receiving a data signal, a control port, and an output;

a second stage having at least two power states, said second stage having an input coupled to the output of said first stage, a control port, and an output capable of passing said signal as amplified by said first and second stages;

an output circuit having at least two impedance matching states, said output circuit having an input coupled to the output of said second stage, a control port, and an output for coupling to a load; and

a state determination circuit coupled to the control port of said first stage for selectively configuring said first stage in one of the at least two power states, coupled to the control port of said second stage for selectively configuring said second stage in one of the at least two power states, and coupled to the control port of said output circuit for selectively configuring said output circuit in one of the at least two impedance matching stages.

14. The amplifier of claim 13, wherein when said state determination circuit configures said first stage in a first of the at least two power states, said second stage in a first of the at least two power states, and said output circuit in a first of the at least two impedance matching states, said amplifier operates at a first power efficiency level; and

wherein when said state determination circuit configures said first stage in a second of the at least two power states, said second stage in a second of the at least two power states, and said output circuit in a second of the at least two impedance matching states, said amplifier operates at a second power efficiency level.

15. The amplifier of claim 14, wherein said state determination circuit selectively configures said first stage, said second stage, and said output circuit based on a signal strength indicator signal generated by the base station.

16. The amplifier of claim 14, wherein said first stage comprises at least:

a first power device; and

a second power device connected in parallel with said first power device.

17. The amplifier of claim 16, wherein said second stage comprises at least:

a third power device; and

a fourth power device connected in parallel with said first power device.

18. The amplifier of claim 17, wherein said state determination circuit selectively configures said first stage by selectively enabling said second power device, said first stage

being in one of the at least two power states when said first and second power devices are enabled and being in another of the at least two power states when said first power device is enabled and said second power device is not enabled; and

wherein said state determination circuit selectively configures said second stage by selectively enabling said fourth power device, said second stage being in one of the at least two power states when said third and fourth power devices are enabled and being in another of the at least two power states when said third power device is enabled and said fourth power device is not enabled.

19. A method for amplifying a signal passing from a source to a load, said method comprising the steps of:

determining an output power level of an amplifier;

configuring a first stage amplifier of the amplifier in one of at least two states based on said determined output power level, said first stage amplifier amplifying said signal; and

configuring a second stage amplifier of the amplifier in one of at least two states based on said determined output power level, said second stage amplifier amplifying said signal as amplified by said first stage amplifier.

20. The method of claim 19, further comprising the step of:

configuring an output matching circuit in one of at least two impedance states based on said determined level, said output matching circuit matching the impedance of said second stage amplifier and the impedance of the load.

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21. The method of claim 20, wherein said step of configuring said first stage amplifier comprises the steps of:

enabling a first power device of said first stage amplifier when said power level is within a first output power range, said first stage amplifier comprising at least said first power device and an enabled second power device, such that said first power device and said second power device are both enabled; and

disabling said first power device when said power level is within a second output power range, such that only said second power device is enabled.

22. The method of claim 21, wherein said step of configuring said second stage amplifier stage comprises the steps of:

enabling a third power device of said second stage amplifier when said power level is within said first output power range, said second stage amplifier comprising at least said third power device and an enabled fourth power device, such that said third power device and said fourth power device are both enabled; and

disabling said third power device when said power level is within said second output power range, such that only said fourth power device is enabled.